THAT WHICH IS CLAIMED IS:

1. A method for forming an ohmic contact to silicon carbide for a semiconductor device, the method comprising:

implanting phosphorus atoms into a surface of an n-type silicon carbide substrate thereby forming a layer on the silicon carbide substrate having an increased concentration of phosphorus;

annealing the implanted silicon carbide substrate; and

depositing a layer of metal on the implanted surface of the silicon carbide that forms an ohmic contact between the phosphorus-implanted silicon carbide and the deposited metal.

2. A method according to claim 1 comprising implanting the phosphorus at room temperature.

3. A method according to claim 1 comprising growing at least one epitaxial layer on a surface of the silicon carbide substrate opposite the implanted surface.

4. A method according to claim 1 wherein the step of growing the epitaxial layer on the silicon carbide substrate follows the step of annealing of the implanted silicon carbide substrate.

5. A method according to claim 1 wherein the first annealing the implanted silicon carbide substrate occurs at a temperature between about 1000°C and 1300°C.

6. A method according to claim 1, wherein the implanted silicon carbide substrate is annealed at a temperature at or above about 1000°C.

7. A method according to claim 1, wherein the implanted silicon carbide substrate is annealed at a temperature at or above about 1300°C.

8. A method according to claim 1 wherein the metal is selected from the group consisting of titanium, aluminum, nickel, silver and platinum.

9. A method according to claim 1 wherein the metal has a work function equal to or lower than the work function of platinum.

10. A method according to claim 1 wherein said implanted phosphorus forms a zone of increased carrier concentration in said silicon carbide substrate.

11. A method according to claim 10 wherein said concentration of phosphorus progressively decreases away from said surface.

12. A method according to claim 10 wherein said concentration of phosphorus is approximately level for a predetermined thickness in said silicon carbide substrate.

13. A method according to claim 10 wherein said zone of increased carrier concentration is at least about 1000 Å thick.

14. A method according to claim 1 comprising implanting phosphorus at a plurality of implant energy levels.

15. A method according to claim 1 comprising implanting phosphorus at an implant energy level of 25 keV at a dose of 10^{15} cm^{-2} or more.

16. A method according to claim 15 further comprising implanting phosphorus at an implant energy level of 50 keV at a dose of 10^{15} cm^{-2} or more.

17. A method according to claim 16 further comprising implanting phosphorus at an implant energy level of 100 keV at a dose of 10^{15} cm^{-2} or more.

18. A semiconductor device comprising:

an n-type silicon carbide substrate having a first surface and a second surface;

at least one epitaxial layer on said first surface of said silicon carbide substrate;

a zone of increasing phosphorus concentration in said silicon carbide substrate and extending from said second surface of said substrate toward said first surface; and

a layer of metal deposited on said second surface of said semiconductor substrate that forms an ohmic contact at the interface of said metal and said zone of increased carrier concentration.

19. A semiconductor device according to claim 18 wherein the initial carrier concentration in said n-type silicon carbide is above about $1x10^{14}$ cm^{-3}.

20. A semiconductor device according to claim 19 wherein the carrier concentration in said zone of increased carrier concentration is between about $1x10^{19}$ and $1x10^{20}$ cm^{-3} and is greater than the carrier concentration in the remainder of said silicon carbide substrate.

21. A semiconductor device according to claim 18 wherein said epitaxial layer is selected from the group consisting of silicon carbide, a group III-nitride; and an oxide of silicon, gallium, aluminum or indium.

22. A semiconductor device according to claim 18 wherein said metal is selected from the group consisting of titanium, aluminum, nickel, silver and platinum.

23. A method according to claim 18 wherein the metal has a work function equal to or lower than the work function of platinum.

24. A semiconductor device comprising:

a silicon carbide substrate having a first surface and a second surface and an initial carrier concentration imparting an n-type conductivity to said substrate;

at least one epitaxial layer on said first surface of silicon carbide substrate;

a zone of increased carrier concentration in said silicon carbide substrate and extending from said second surface of said silicon carbide substrate toward said first surface, said zone being characterized by a concentration of phosphorus that progressively decreases from said second surface toward said first surface; and

an ohmic contact on said second surface of said silicon carbide substrate.

25. A semiconductor device according to claim 24 wherein the initial carrier concentration in said silicon carbide substrate is above about $1x10^{14}$ cm^{-3}.

26. A semiconductor device according to claim 25 wherein the carrier concentration in the zone of increased carrier concentration is between about $1x10^{19}$ and $1x10^{20}$ cm^{-3} and is greater than the carrier concentration in the remainder of said silicon carbide substrate.

27. A semiconductor device according to claim 24 wherein said epitaxial layer is selected from the group consisting of silicon carbide, a group III-nitride; and an oxide of silicon, gallium, aluminum or indium.

28. A light emitting diode comprising:

an n-type silicon carbide substrate having respective first and second surfaces;

a Group III nitride active region on said first surface said substrate;

an epitaxial layer on said active region;

a zone of increased carrier concentration in said silicon carbide substrate and extending from said second surface of said silicon carbide substrate toward said first surface;

an ohmic contact on said second surface of said substrate; and

an ohmic contact on said epitaxial layer.

29. A light emitting diode according to claim 28, wherein said zone of increased carrier concentration is characterized by a concentration of phosphorus that progressively decreases from said second surface toward said first surface.

30. A light emitting diode according to claim 28 wherein said active region comprises a structure selected from the group consisting of homojunctions, single heterojunctions, double heterojunctions, superlattices and quantum wells.

31. A light emitting diode according to claim 30 wherein one or more portions of said structure are selected from the group consisting of gallium nitride, aluminum nitride, indium nitride, aluminum gallium nitride, indium gallium nitride, aluminum indium nitride and aluminum indium gallium nitride.

32. A light emitting diode according to Claim 28 wherein said active region is selected from the group consisting of gallium nitride, aluminum nitride, indium nitride, aluminum gallium nitride, indium gallium nitride, aluminum indium nitride and aluminum indium gallium nitride.

33. A light emitting diode according to claim 28 wherein said ohmic contact to said substrate is selected from the group consisting of titanium, aluminum, nickel, silver and platinum.